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PATENT AND TRADEMARK OFFICE

APPLICANTS:	Steven G. Roskowski, Dean M. Drako and William T. Krein
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TITLE:	SYSTEM FOR RECEIVING A CONTROL SIGNAL FROM A DEVICE FOR SELECTING ITS ASSOCIATED CLOCK SIGNAL FOR CONTROLLING THE TRANSFERRING OF INFORMATION VIA A BUFFER
EXAMINER:	Tammara R. Peyton
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STATEMENT OF SUBSTANCE OF EXAMINER INTERVIEW

SIR:

On January 30, 2008, the Examiner and the undersigned attorney discussed claims 26, 28, and 29 over the phone. The undersigned attorney suggested making the following changes in an Examiner's Amendment:

26. A method of transferring data between a first component and a second component in a computer system, the first component clocked by a first clock signal, and the second component clocked by a second clock signal, comprising:

clocking data from the first component to a buffer via a data path using the first clock signal in the absence of a valid signal from the ~~first~~ second component, the first component always using the first clock signal to transfer data from the first component to the buffer without synchronizing the transfer of the data to another clock;

clocking data from the buffer to the second component via the data path using the second clock signal in response to the valid signal from the second component without transferring other data to the buffer; and

supplying the first and second clock signals to the buffer via a multiplexer having a plurality of inputs and an output coupled to the buffer, the inputs for receiving the first and second clock signals and [[a]] the valid signal from the second component, the multiplexer supplying the second clock signal to the buffer in response to the valid signal;

wherein the timing of the first clock signal is independent of the timing of the second clock signal.

28. An apparatus for use in a computer system for transferring data between a plurality of components including at least one source component and at least one destination component, the source component clocked by a first clock signal, and the destination component clocked by a second clock signal, comprising:

a buffer coupled to the source component and the destination component via a data path, the source component always using the first clock signal to transfer data from the source component to the buffer without synchronizing the transfer of the data to another clock;

a multiplexer having inputs coupled to the first clock signal and the second clock signal, and an output coupled to the buffer, the multiplexer supplying the first clock signal to the buffer to clock data from the source component to the buffer via the data path in the absence of a gate signal from the destination component, the multiplexer supplying the second clock signal to the buffer to clock data from the buffer to the destination component via the data path in response to the gate signal from the destination component without transferring other data to the buffer; and

a broadcast bus coupled to the source component, the destination component and the buffer, the broadcast bus for transferring a ready signal from the source component to the destination component indicating that the transfer of data from the ~~first~~ source component to the buffer is complete;

wherein the timing of the first clock signal is independent of the timing of the second clock signal.

29. The apparatus of claim 28, wherein the source component places the address of the destination component on the broadcast bus and the destination component ~~supplying~~ supplies the gate signal to the multiplexer in response to the address.

The undersigned attorney explained that these amendments merely correct typographical errors and do not change the scope of the claims.

The Examiner agreed and said that she would issue a Supplemental Notice of Allowability, which would include the above amendments as an Examiner's Amendment.

Respectfully submitted,
STEVEN G. ROSKOWSKI,
ET AL.

Dated: January 30, 2008

By: /Sabra-Anne R. Truesdale/

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